What is Claimed is:

1. An apparatus for processing a bit stream, comprising:

a circular buffer for storing a transmitted bit stream;

a first register for storing data indicating a first read point of the bit stream stored in the circular buffer;

a first backup register for backing up the data stored in the first register;

a second register for storing data indicating a number of bits to be read from the circular buffer;

a third register for storing data indicative of the number of bits to be ignored from the read point;

a second backup register for backing up the data stored in the third register;

an adder for adding the data stored in the second register and the data stored in the third register; and

a controller responsive to the adder to determine a number of bits to be shifted to read desired data from the circular buffer.

2. An apparatus as defined in claim 1, further comprising:

a fourth register for storing data indicating an address of the circular buffer where the transmitted bit stream is to be stored;

a fifth register for storing data retrieved from a first memory word in the circular buffer located adjacent a second memory word identified by the first read point;

a third backup register for backing up the data stored in the fifth register;

a shifter for shifting data from the second memory word and data from the first memory word by the number of bits determined by the controller; and

a masking circuit for masking unwanted bits.

3. An apparatus as defined in claim 2, wherein the apparatus has a first read mode and a second read mode.

4. An apparatus as defined in claim 3, wherein, in the first read mode, the data in the first, the second, and the third backup registers is updated simultaneously with the corresponding one of the first, the third and the fifth registers.

5. An apparatus as defined in claim 4, wherein, in the second read mode, the data in the first, the second, and the third backup registers is not updated when the data in the corresponding one of the first, the third and the fifth registers is updated.

6. An apparatus as defined in claims 2 wherein the masking circuit identifies the unwanted bits based upon the data stored in the second register.

7. An apparatus for reading data from a circular buffer storing data in a plurality of memory words, comprising:

a first storage device for storing data indicative of a desired number of bits to be read;

a second storage device for storing data indicative of a first bit to be read in a first memory word;

a shifter for receiving data stored in the first memory word and data stored in the second memory word located adjacent the first memory word in the circular buffer; and

a logic circuit in communication with the first and second storage devices for controlling the shifter to shift a number of bits specified by the data in the first and second storage devices to align the data in the shifter in a read position.

8. An apparatus as defined in claim 7 wherein the logic circuit comprises:

an adder for summing the data stored in the first and second storage devices to develop a sum; and

a controller for subtracting the sum from a predetermined number to develop the number of bits to be shifted by the shifter.

9. An apparatus as defined in claim 8 wherein the predetermined number is 32.

10. An apparatus as defined in claim 7 further comprising:

a third storage device for storing data indicative of the first memory word containing data to be read; and

a fourth storage device for storing data contained in the second memory word.

11. An apparatus as defined in claim 7 further comprising a masking circuit for masking unwanted bits output by the shifter.

12. An apparatus for reading data from a circular buffer storing data in a plurality of memory words, comprising:

a first masking circuit for receiving data contained in at least two memory words of the circular buffer, the at least two memory words including data to be read, wherein, when a rightmost bit of the received data is not part of the data to be read, the first masking circuit outputs a subset of the received

data which includes at least the data to be read but excludes at least the rightmost bit; and

a second masking circuit for masking unwanted bits from the output of the first masking circuit.

13. An apparatus as defined in claim 12 wherein the first masking circuit comprises a shifter, and the shifter develops the subset by shifting the received data until the rightmost bit contains data to be read.

14. An apparatus as defined in claim 12 wherein the second masking circuit masks unwanted bits by zeroing all bits to the left of the data to be read.

15. A method of reading data from a circular buffer storing data in a plurality of memory words, comprising the steps of:

identifying at least one of the memory words containing data to be read;

identifying a number of bits to be read;

identifying a first bit to be read;

retrieving all data in the memory words of the circular buffer storing data to be read;

inputting the retrieved data to a shifter;

summing the number of bits to be read with a number of bits to be ignored adjacent the first bit to be read to develop a sum;

subtracting the sum from a predetermined number to determine a shift amount;

shifting the data in the shifter by the shift amount to remove unwanted bits adjacent a last bit to be read;

masking unwanted bits adjacent the first bit to be read; and

outputting the bits to be read.

16. A method as defined in claim 15 wherein the bits to be ignored are in front of the first bit to be read.

17. A method as defined in claim 15 wherein the masked unwanted bits are in front of the first bit to be read.